Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 11, 38 and 42 as follows:

Listing of Claims:

1. (Currently Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of opposed lateral edges;

at least one electrically conductive external terminal;

an interposer having a die attach surface and an external surface opposite of the die attach surface disposed in between the semiconductor die and the at least one external terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed between the semiconductor die and the interposer, each strip being mutually independently positionable, with a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges of the semiconductor die, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the interposer.

2. (Original) The package of claim 1, further comprising an encapsulating material substantially filling regions remaining in between the semiconductor die and the interposer.

3. (Original) The package of claim 1 wherein the interposer comprises a flexible material.

4-7. (Canceled)

8. (Original) The package of claim 1 wherein the at least one electrically conductive external terminal comprises a solder ball.

9. (Previously Presented) The package of claim 1 wherein the plurality of strips of compliant adhesive film comprise strips of compliant adhesive film positioned in parallel along a longitude of the semiconductor die.

10. (Previously Presented) The package of claim 1 wherein a first and a second of the plurality of strips of compliant adhesive film are positioned at a right angle with respect to each other.

11. (Currently Amended) A device package assembly for a semiconductor die being constructed from a process comprising:

laminating a plurality of strips of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer being formed of an organic substrate or a polyimide substrate and further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first length being substantially

greater than the second length, each strip being mutually independently positionable, with the strips extending substantially the entire distance between the first pair of opposed lateral edges, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, the plurality of adhesive film strips being further operable to reduce a thermal mismatch stress between the semiconductor die and the interposer; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

12. (Original) The package assembly of claim 11 wherein the process further comprises substantially filling regions remaining in between the semiconductor die and the interposer with an encapsulating material.

13. (Original) The package assembly of claim 11 wherein the process further comprises attaching an external terminal to the at least one electrically conductive interconnect adjacent to the external surface of the interposer.

14. (Original) The package assembly of claim 13 wherein the external terminal comprises a solder ball.

15. (Original) The package assembly of claim 11 wherein the interposer comprises a flexible material.

16-17. (Canceled)

18. (Previously Presented) The package assembly of claim 11 wherein the plurality of strips of compliant adhesive film comprise strips of film positioned in parallel along a longitude of the semiconductor die.

19-37. (Canceled)

38. (Currently Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die, each strip being mutually independently positionable, with a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the interposer.

39. (Canceled)

40. (Previously Presented) The semiconductor device package of claim 38 wherein the strips of compliant adhesive film comprise strips of compliant adhesive material positioned in parallel with a longitude of the semiconductor die.

41. (Previously Presented) The semiconductor device package of claim 38, further comprising an external conductive terminal electrically coupled to the electrically conductive interconnect and positioned on a surface of the interposer opposite of the die attach surface.

42. (Currently Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the carrier layer to the die attach surface of the interposer, each strip being mutually independently positionable, with a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips of compliant adhesive film further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die, the plurality of adhesive film strips being operable to reduce a thermal mismatch stress between the semiconductor die and the interposer.

43. (Previously Presented) The semiconductor device package of claim 42 wherein the strips of compliant adhesive film are positioned substantially parallel with a longitude of the semiconductor die.

44. (Previously Presented) The semiconductor device package of claim 42 wherein a first and a second strip of the plurality are positioned substantially at a right angle with respect to each other.

45. (Previously Presented) The semiconductor device package of claim 42 wherein at least one of the plurality of strips comprises a compliant carrier layer and at least one adhesive layer adhered to the compliant carrier layer.

46-49. (Canceled)

50. (Previously Presented) The semiconductor device package of claim 1, wherein the carrier layer is further comprised of multiple layers.

51. (Previously Presented) The device package assembly process of claim 11, wherein the carrier layer is further comprised of multiple layers.

52. (Previously Presented) The semiconductor device package of claim 38, wherein the carrier layer is further comprised of multiple layers.

53. (Previously Presented) The semiconductor device package of claim 42, wherein the carrier layer is further comprised of multiple layers.